

CLAIMS

We Claim:

1 1. An isolated analog-to-digital converter system having at
2 least two channels, said isolated analog-to-digital converter
3 system comprising:

4 first and second analog-to-digital converters for receiving
5 respective analog input signals and outputting respective digital
6 data signals; and

7 first and second calibration resistors coupled to the
8 respective outputs of the first and second analog-to-digital
9 converters, for use in calibrating relative gain of the first and
10 second analog-to-digital converters wherein relative gain of the
11 first and second analog-to-digital converters is calibrated from
12 the ratio of the resistances of the first and second calibration
13 resistors.

1 2. The isolated analog-to-digital converter system of claim
2 1, wherein the first and second analog-to-digital converters each
3 further include:

4 an on-chip CMOS bandgap reference calibrated with the matched
5 inputs from the first and second calibration resistors,
6 respectively.

1 3. The isolated analog-to-digital converter system of claim
2 2, further comprising:

3 wherein the first and second calibration resistors comprise a
4 pair of matched precision resistors.

1 4. The isolated analog-to-digital converter system of claim
2 3, further comprising:

3 a data receiving device, coupled to the first and second
4 analog converters, for receiving data from the first and second
5 analog-to-digital converters.

1 5. The isolated analog-to-digital converter system of claim
2 4, further comprising:

3 first and second isolation transformers, each coupled between
4 a respective first and second analog-to-digital converter and the
5 data receiving device, for isolating the data receiving device from
6 the first and second analog-to-digital converters.

1 6. The isolated analog-to-digital converter system of claim
2 5, further comprising:

3 a current limiting/isolating resistor, coupled between the
4 first and second analog-to-digital converters, for limiting overall
5 current and isolate the first and second calibrations resistors
6 from one another.

1 7. The isolated analog-to-digital converter system of claim
2 6, wherein the first and second analog-to-digital converters are
3 referenced to respective local grounds GND1 and GND2 having
4 independent potentials.

5 8. The isolated analog-to-digital converter system of claim
6 7, wherein the first and second calibration resistors are on a
common substrate which has good thermal conduction and electrical
insulation characteristics.

1 9. The isolated analog-to-digital converter system of claim
2 8, wherein each of the first and second analog-to-digital
3 converters are on respective semiconductor chips, each
4 semiconductor chip provided with silicon thermal meters,
5 wherein the isolated analog-to-digital converter system is
6 subject to a two-temperature factory calibration.

1 10. The isolated analog-to-digital converter system of claim
2 2, wherein

3 said first and second calibration resistors carry
4 substantially the same current, with the first and second analog-
5 to-digital converters drawing substantially no current from the
6 first and second calibration resistors, such that the first and
7 second calibration resistors provide a pair of ratio matched
8 voltages for the calibration of the CMOS bandgap references in the
9 respective first and second analog-to-digital converters.

10 11. The isolated analog-to-digital converter system of claim
11 10, wherein, after initial testing calibration, the gains of the
12 first and second analog-to-digital converters are known, and the
13 first and second analog-to-digital converters measure and record
14 the ratio $R1/R2$ of the first and second calibration resistors to
15 one another such that in field operation with the ratio of $R1/R2$
16 assumed to be unchanged, the first and second analog-to-digital
17 converters measure the ratio $R1/R2$ and gain of one of the first and
18 second analog-to-digital converters is adjusted to match the other
19 of the first and second analog-to-digital converters.

1 12. A method of automatically calibrating relative gains of
2 an at least two channel isolated analog-to-digital converter system
3 including first and second analog-to-digital converters for
4 receiving respective analog input signals and outputting respective
5 digital data signals, said method comprising the steps of:

6 providing first and second calibration resistors coupled to
7 the respective outputs of the first and second analog-to-digital
8 converters, respectively, and

9 calibrating relative gain of the first and second analog-to-
10 digital converters from the ratio of the resistances of the first
11 and second calibration resistors.

12 13. The method of claim 12, wherein the first and second
13 analog-to-digital converters each further include respective on-
14 chip CMOS bandgap references, and said step of calibrating relative
15 gain of the first and second analog-to-digital converters comprises
16 the steps of calibrating the respective CMOS bandgap references
17 with matched inputs from the first and second calibration
18 resistors.

1 14. The method of claim 13, the step of providing first and
2 second calibration resistors further comprises the step of
3 providing a pair of matched precision resistors.

1 15. The method of claim 14, further comprising the step of:
2 receiving, in a data receiving device, coupled to the first
3 and second analog converters, data from the first and second
4 analog-to-digital converters.

1 16. The method of claim 15, further comprising the step of:
2 isolating the first and second analog-to-digital converters
3 from the data receiving device, using respective first and second
4 isolation transformers coupled between respective first and second
5 analog-to-digital converters and the data receiving device.

1 17. The method of claim 16, further comprising the step of:
2 limiting overall current through the first and second
3 calibration resistors and isolating the first and second
4 calibration resistors from one another by providing a current
5 limiting/isolating resistor, coupled between the first and second
6 analog-to-digital converters.

1 18. The method of claim 17, wherein the first and second
2 analog-to-digital converters are referenced to respective local
3 grounds GND1 and GND2 having independent potentials.

1 19. The method of claim 18, wherein the step of providing the
2 first and second calibration resistors further comprises the step
3 of providing the first and second calibration resistors on a common
4 substrate which has good thermal conduction and electrical
5 insulation characteristics.

1 20. The method of claim 19, wherein each of the first and
2 second analog-to-digital converters are on respective semiconductor
3 chips, each semiconductor chip provided with silicon thermal
4 meters, said method further comprising the step of

5 calibrating the respective gains of the first and second
6 analog-to-digital converters with a two-temperature factory
7 calibration.

1 21. The method of claim 13, wherein the first and second
2 calibration resistors carry substantially the same current, with

3 the first and second analog-to-digital converters drawing
4 substantially no current from the first and second calibration
5 resistors, such that the first and second calibration resistors
6 provide a pair of ratio matched voltages for the calibration of the
7 CMOS bandgap references in the respective first and second analog-
8 to-digital converters.

10 22. The method of claim 21, wherein after initial testing
11 calibration, the gains of the first and second analog-to-digital
12 converters are known, said method further comprising the steps of:

13 measuring, using the first and second analog-to-digital
14 converters, the ratio $R1/R2$ of the first and second calibration
15 resistors to one another,

1 recording, using the first and second analog-to-digital
2 converters, the ratio $R1/R2$ of the first and second calibration
3 resistors to one another,

4 measuring, using the first and second analog-to-digital
5 converters, in a subsequent field calibration, assuming the ratio
6 of $R1/R2$ is unchanged, the ratio $R1/R2$, and

7 adjusting the gain of one of the first and second analog-to-
8 digital converters to match the other of the first and second
9 analog-to-digital converters.

1 23. A power measuring system for measuring power current,
2 comprising:

3 an isolated analog-to-digital converter system having at least
4 two channels, said isolated analog-to-digital converter system
5 comprising:

6 first and second analog-to-digital converters for
7 receiving respective analog input signals and outputting
8 respective digital data signals; and

9 first and second calibration resistors coupled to the
10 respective outputs of the first and second analog-to-digital
11 converters, for use in calibrating relative gain of the first
12 and second analog-to-digital converters wherein relative gain
13 of the first and second analog-to-digital converters is
14 calibrated from the ratio of the resistances of the first and
15 second calibration resistors.

1 24. The power measuring system of claim 23, wherein the first
2 and second analog-to-digital converters each further include:

3 an on-chip CMOS bandgap reference calibrated with the matched
4 inputs from the first and second calibration resistors,
5 respectively.

1 25. The power measuring system of claim 24, further
2 comprising:

3 wherein the first and second calibration resistors comprise a
4 pair of matched precision resistors.

1 26. The power measuring system of claim 25, further
2 comprising:

3 a data receiving device, coupled to the first and second
4 analog converters, for receiving data from the first and second
5 analog-to-digital converters.

6 27. The power measuring system of claim 26, further
comprising:

1 first and second isolation transformers, each coupled between
2 a respective first and second analog-to-digital converter and the
3 data receiving device, for isolating the data receiving device from
4 the first and second analog-to-digital converters.

1 28. The power measuring system of claim 27, further
2 comprising:

3 a current limiting/isolating resistor, coupled between the
4 first and second analog-to-digital converters, for limiting overall
5 current and isolate the first and second calibrations resistors
6 from one another.

1 29. The power measuring system of claim 28, wherein the first
2 and second analog-to-digital converters are referenced to
3 respective local grounds GND1 and GND2 having independent
4 potentials.

1 30. The power measuring system of claim 29, wherein the first
2 and second calibration resistors are on a common substrate which
3 has good thermal conduction and electrical insulation
4 characteristics.

1 31. The power measuring system of claim 30, wherein each of
2 the first and second analog-to-digital converters are on respective
3 semiconductor chips, each semiconductor chip provided with silicon
4 thermal meters,

5 wherein the isolated analog-to-digital converter system is
6 subject to a two-temperature factory calibration.

1 32. The power measuring system of claim 24, wherein
2 said first and second calibration resistors carry
3 substantially the same current, with the first and second analog-
4 to-digital converters drawing substantially no current from the
5 first and second calibration resistors, such that the first and
6 second calibration resistors provide a pair of ratio matched
7 voltages for the calibration of the CMOS bandgap references in the
8 respective first and second analog-to-digital converters.

9 33. The power measuring system of claim 32, wherein, after
10 initial testing calibration, the gains of the first and second
11 analog-to-digital converters are known, and the first and second
12 analog-to-digital converters measure and record the ratio $R1/R2$ of
13 the first and second calibration resistors to one another such that
14 in field operation with the ratio of $R1/R2$ assumed to be unchanged,
15 the first and second analog-to-digital converters measure the ratio
16 $R1/R2$ and gain of one of the first and second analog-to-digital
17 converters is adjusted to match the other of the first and second
18 analog-to-digital converters.